IN THE CLAIMS

Please amend claims 31, 34, 37-38, 41, and 44 as follows below.

Please add new claims 52-55 as follows below.

The following listing of claims replaces all prior versions, and listings of claims in the application.

MARKED UP CLAIMS LISTING

1-30. (Cancelled)

31. (Currently Amended) A memory control translator comprising:

a first bus interface for a first memory interface, the first bus interface to couple to a memory control unit;

a second bus interface for a second memory interface, the second bus interface to couple to a system memory, the second memory interface differing from the first memory interface;

a command decoder and generator coupled between the first bus interface and the second bus interface, the command decoder and generator to decode and translate commands for the first memory interface from the memory control unit into commands for the second memory interface;

at least one data buffer coupled between the first bus interface and the second bus interface, the at least one data buffer to store data;

at least one address buffer coupled between the first bus interface and the second bus interface, the at least one address buffer to store one or more addresses corresponding to memory locations associated with the data stored in the at least one data buffer;

and wherein the memory control translator to synchronize commands, data and addresses between the memory control unit and the system memory to send a buffered write command and its corresponding write data to the system memory for execution upon receipt of another write command from the memory control unit, without waiting for write data associated with the another write command to arrive from the memory control unit.

32. (Previously Presented) The memory control translator of claim 31, wherein

the at least one data buffer is a first FIFO buffer.

33. (Previously Presented) The memory control translator of claim 32, wherein

the at least one address buffer is a second FIFO buffer.

34. (Currently Amended) The memory control translator of claim 31, wherein

the at least one data buffer includes

a write data buffer ~~for writing~~ to write data into memory, and

a read data buffer ~~for reading~~ to read data from memory.

35. (Previously Presented) The memory control translator of claim 34, wherein

the at least one address buffer includes

a column address buffer to store column addresses, and

a row address buffer to store row addresses.

36. (Previously Presented) The memory control translator of claim 31, wherein

the first memory interface is an RDRAM memory interface, and

the second memory interface is an SDRAM memory interface.

37. (Currently Amended) A [[The]] memory control translator ~~of claim 31 further~~ comprising:

a first bus interface for a first memory interface, the first bus interface to couple to a memory control unit;

a second bus interface for a second memory interface, the second bus interface to couple to a system memory, the second memory interface differing from the first memory interface;

a command decoder and generator coupled between the first bus interface and the second bus interface, the command decoder and generator to decode and translate

commands for the first memory interface from the memory control unit into commands for the second memory interface;

at least one data buffer coupled between the first bus interface and the second bus interface, the at least one data buffer to store data;

at least one address buffer coupled between the first bus interface and the second bus interface, the at least one address buffer to store one or more addresses corresponding to memory locations associated with the data stored in the at least one data buffer; and

read bypass logic including

at least one address comparator to compare an address from the memory control unit with an address stored in the at least one address buffer, and

a multiplexor coupled to the at least one address comparator and the at least one data buffer, the multiplexor to select data from the at least one data buffer in response to the at least one address comparator;

wherein the memory control translator to synchronize commands, data and addresses between the memory control unit and the system memory.

38. (Currently Amended) The memory control translator of claim 37, wherein

the at least one data buffer includes

a write data buffer ~~for writing~~ to write data into memory, and

a read data buffer ~~for reading~~ to read data from memory,

and

the multiplexor to select data from the write data buffer in response to the at least one address comparator.

39. (Previously Presented) The memory control translator of claim 38, wherein

the at least one address buffer includes

a column address buffer to store column addresses, and

a row address buffer to store row addresses,

the at least one comparator includes

a column address comparator to compare column addresses, and

a row address comparator to compare row addresses, and

the multiplexor to select data from the write data buffer in response to the column address comparator and the row address comparator.

40. (Previously Presented) The memory control translator of claim 36, wherein

the system memory is SDRAM memory and the memory control unit generates commands for RDRAM memory.

41. (Currently Amended) A memory control translator comprising:

an RDRAM memory interface to couple to a memory control unit;

an SDRAM memory interface to couple to a system memory, the SDRAM memory interface differing from the RDRAM memory interface;

a command decoder and generator coupled between the RDRAM memory interface and the SDRAM memory interface, the command decoder and generator to decode and translate commands received by the RDRAM memory interface from the memory control unit into commands to transmit out over the SDRAM memory interface to the system memory;

at least one data buffer coupled between the RDRAM memory interface and the SDRAM memory interface, the at least one data buffer to store data;

at least one address buffer coupled between the RDRAM memory interface and the SDRAM memory interface, the at least one address buffer to store one or more addresses corresponding to memory locations associated with the data stored in the at least one data buffer;

and wherein the memory control translator to synchronize commands, data and addresses between the memory control unit and the system memory to send a buffered write command and its corresponding write data to the system memory for execution upon receipt of another write command from the memory control unit, without waiting for write data associated with the another write command to arrive from the memory control unit.

42. (Previously Presented) The memory control translator of claim 41, wherein
the at least one data buffer is a first FIFO buffer.

43. (Previously Presented) The memory control translator of claim 42, wherein
the at least one address buffer is a second FIFO buffer.

44. (Currently Amended) The memory control translator of claim 41, wherein
the at least one data buffer includes
a write data buffer ~~for writing~~ to write data into memory, and
a read data buffer ~~for reading~~ to read data from memory.

45. (Previously Presented) The memory control translator of claim 44, wherein
the at least one address buffer includes
a column address buffer to store column addresses, and
a row address buffer to store row addresses.

46. (Previously Presented) The memory control translator of claim 41, wherein

the system memory is SDRAM memory and the memory control unit generates commands for RDRAM memory, and

the command decoder and generator translates commands for RDRAM memory into commands for the SDRAM memory.

47. (Previously Presented) A memory control translator comprising:

an RDRAM memory interface to couple to a memory control unit;

an SDRAM memory interface to couple to a system memory, the SDRAM memory interface differing from the RDRAM memory interface;

a command decoder and generator coupled between the RDRAM memory interface and the SDRAM memory interface, the command decoder and generator to decode and translate commands received by the RDRAM memory interface from the memory control unit into commands to transmit out over the SDRAM memory interface to the system memory;

a write data buffer coupled between the RDRAM memory interface and the SDRAM memory interface, the write data buffer to store data to be written into the system memory, and

a read data buffer coupled between the RDRAM memory interface and the SDRAM memory interface, the read data buffer to store data to be read from the system memory;

a column address buffer coupled between the RDRAM memory interface and the SDRAM memory interface, the column address buffer to store one or more column addresses corresponding to memory locations associated with the data

stored in the write data buffer and the read data buffer; and

a row address buffer coupled between the RDRAM memory interface and the SDRAM memory interface, the row address buffer to store one or more row addresses corresponding to the memory locations associated with the data stored in the write data buffer and the read data buffer.

48. (Previously Presented) The memory control translator of claim 47, wherein

the memory control translator to synchronize commands, data and addresses between the memory control unit and the system memory.

49. (Previously Presented) The memory control translator of claim 47, wherein

the system memory is SDRAM memory and the memory control unit generates commands for RDRAM memory, and

the command decoder and generator translates commands for RDRAM memory into commands for the SDRAM memory.

50. (Previously Presented) The memory control translator of claim 47, wherein

the write data buffer is a first FIFO buffer, and

the read data buffer is a second FIFO buffer.

51. (Previously Presented) The memory control translator of claim 50, wherein

the column address buffer is a third FIFO buffer, and the row address buffer is a fourth FIFO buffer.

52. (New) The memory control translator of claim 41 further comprising:

read bypass logic coupled to the at least one data buffer and the at least one address buffer, the read bypass logic to determine if a read address associated with a read command from the memory control unit matches a buffered write address stored in the at least one address buffer and if there is a match, the buffered write data associated with the buffered write address is used as read data for the read command having the matching read address.

53. (New) The memory control translator of claim 52, wherein

the read bypass logic includes

at least one address comparator to compare an address from the memory control unit with an address stored in the at least one address buffer, and

a multiplexor coupled to the at least one address comparator and the at least one data buffer, the multiplexor to select data from the at least one data buffer in response to the at least one address comparator.

54. (New) The memory control translator of claim 47 further comprising:

read bypass logic coupled to the write data buffer, the column address buffer, and the row address buffer, the read bypass logic to determine if a read address associated with a read command from the memory control unit matches a buffered write address stored in the row address buffer and the column address buffer and if there is a match, the buffered write data associated with the buffered write address is used as read data for the read command having the matching read address.

55. (New) The memory control translator of claim 54, wherein

the read bypass logic includes

a row address comparator to compare a row address from the memory control unit with a row address stored in the row address buffer,

a column address comparator to compare a column address from the memory control unit with a column address stored in the column address buffer, and

a multiplexor coupled to the row address comparator, the column address comparator and the write buffer, the multiplexor to select data from the write data buffer in response to the row address comparator and the column address comparator.